Paper No. 20

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JICHENG YANG

Appeal No. 2003-1233
Application No. 09/420,817

ON BRIEF

Before WALTZ, JEFFREY T. SMITH and MOORE, ***Administrative Patent Judges***.

JEFFREY T. SMITH, ***Administrative Patent Judge.***

DECISION ON APPEAL

Applicant appeals the decision of the Primary Examiner finally rejecting claims 21 to 29 and 39 to 47.[1] We have jurisdiction under 35 U.S.C. § 134.

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[1] In rendering our decision, we have considered Appellant's arguments presented in the Brief, filed October 29, 2002.

CITED PRIOR ART

As evidence of unpatentability, the Examiner relies on the following references:

Hamzehdoost et al. (Hamzehdoost)	5,689,091	Nov. 18, 1997
Egawa	6,229,215	May 08, 2001 (filed October 23, 1998)
Bertin et al. (Bertin)	6,300,687	Oct. 09, 2001 (filed June 26, 1998)

The Examiner has rejected claims 21 to 29 and 39 to 47 as unpatentable under 35 U.S.C. § 103(a) as obvious over the combination of Egawa, Bertin and Hamzehdoost. (Answer, p. 3).

Rather than reiterate the conflicting viewpoints advanced by the Examiner and Appellant concerning the above-noted rejections, we refer to the Answer and the Brief.

DISCUSSION

We have carefully reviewed the claims, specification and applied prior art, including all of the arguments advanced by both the Examiner and Appellant in support of their respective positions. This review leads us to conclude that the Examiner's § 103 rejection is well founded.

Appellant's invention is directed to multi-chip modules for coupling more than one chip together in a single package. According to the specification, pages 1 and 2, there is a

need for packages which comprise multiple chips that have been connected together prior to connection to the outside world. Claim 24, which is representative of the claimed invention, appears below:

> 24. A multi-chip module comprising:
>
> a central support layer having a central aperture, a top side and a bottom side, a bonding pad on each of said sides and conductive interconnections extending through said layer;
>
> a first chip wire bonded to the top side of said layer through said aperture and secured to the bottom side of said layer;
>
> a second chip secured to the top side of said layer, said second ship secured by bumps to said layer; and
>
> said layer extending outwardly beyond said first and second chips, said layer including a solder ball pad on an extension extending outwardly beyond said first and second chips for electrically connecting said chips to external devices.

Appellant has indicated that "all of the pending claims may be grouped with claim 24." (Brief, p. 5). We interpret Appellant's statement as indicating that all of the claims stand or fall together. Accordingly, all the claims will stand or fall together, and we select claim 24 as representative of the rejected claims. Note ***In re King***, 801 F.2d 1324, 1325, 231 USPQ 136, 137 (Fed. Cir. 1986); ***In re Sernaker***, 702 F.2d 989, 991, 217 USPQ 1, 3 (Fed. Cir. 1983). 37 CFR § 1.192 (c)(7) and (8) (2001).

We have carefully reviewed the claims, specification and applied prior art, including all of the arguments advanced by both the Examiner and Appellant in support of their respective positions. This review leads us to conclude that the Examiner's § 103 rejection is well founded. ***See In re Oetiker***, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992); ***In re Piasecki,*** 745 F.2d 1468, 1471-1472, 223 USPQ 785, 787-788 (Fed. Cir. 1984). We affirm primarily for the reasons advanced by the Examiner and add the following primarily for emphasis.

The Examiner has found that Egawa discloses a semiconductor package, figure 3, that differs from the subject matter of claim 24 in that the first chip is not wire bonded to the top side of the laminate layer. According to the Examiner, Bertin discloses a semiconductor package, figure 8, that contains a chip that is wire bonded to a laminate layer for electrical coupling. The Examiner also found Egawa and Bertin were from the same field of endeavor. The Examiner determined that it would have been obvious to a person of ordinary skill in the art to use wire bonding techniques for electrically connecting the first chip to the laminate layer of Egawa. (Answer, p. 4).

Appellant argues that the Examiner's rejection is based on improper hindsight and there is no motivation or suggestion to modify Egawa with Bertin. (Brief, p. 5). We are not convinced by Appellant's argument. A person having ordinary skill in the art would

have recognized that the wire bonding techniques could have been used in Egawa's semiconductor package. In an alternative embodiment Egawa discloses wire bonding of the top layer of a chip to a central layer. (See figure 1(b)). A person having ordinary skill in the art would have also recognized that the wire bonding could have occurred through the central aperture described in figure 3. (Note Bertin figure 8). It is well settled that the prior art references stand for all of the specific teachings thereof as well as the inferences one of ordinary skill in this art would have reasonably been expected to draw therefrom, see ***In re Fritch,*** 972 F.2d 1260, 1264-65, 23 USPQ2d 1780, 1782-83 (Fed. Cir. 1992); ***In re Preda,*** 401 F.2d 825, 826, 159 USPQ 342, 344 (CCPA 1968).

Appellant argue that Egawa's use of a flip chip design is a teaching away from using wire bonding. (Brief, pp. 5-6). We disagree. The central layer of Egawa's semiconductor package contains connection points on both sides. (See figure 3, points 18 and 32). A person of ordinary skill in the are would have recognized that if the circuitry of the central layer, from the side not facing the first chip, were needed on the first chip wire bonding would have been a suitable connection method.

Appellant argues that Egawa filled the space between the chips 11, 17 and the substrate 30 with a resin 33 for encapsulation and that the hole 31 is not suitable for wire connection. (Brief, p. 6). We disagree. Egawa discloses that the use of wire bonding and

resin encapsulation was known by persons of ordinary skill in the art. (Col. 1, ll. 10-20). Bertin discloses wire bonding of a semiconductor package through a central hole to connect a chip to the central layer. (Figure 8). Thus, a person of ordinary skill in the art would have known the proper techniques for the use of wire bonding through a central aperture.

Based on our consideration of the totality of the record before us, having evaluated the ***prima facie*** case of obviousness in view of Appellant's arguments, we conclude that the subject matter of claims 21 to 29 and 39 to 47 would have been obvious to a person of ordinary skill in the art from the combined teachings of the cited prior art for the reasons stated above and in the Answer.[2]

CONCLUSION

The rejection of claims 21 to 29 and 39 to 47 under 35 U.S.C. § 103(a) as obvious over the combination of Egawa, Bertin and Hamzehdoost is affirmed.

[2] Since Appellant indicated that issues of patentability should be determined based upon claim 24, we have not provided a discussion of the Hamzehdoost reference. The Examiner applied the teachings of this reference for elements of other claims.

Time for taking action

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

THOMAS A. WALTZ ***Administrative Patent Judge***	)
JEFFREY T. SMITH ***Administrative Patent Judge***	) **BOARD OF PATENT APPEALS AND INTERFERENCES**
JAMES T. MOORE ***Administrative Patent Judge***	)

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